CLAIMS:

1. A method of effectively extracting a clock signal from a data stream, comprising the steps of:

generating a plurality of multiphase clock signals;

selecting one of the multiphase signals based on a plurality of synchronization states identifying which of the multiphase clock signals is most closely aligned with the data stream; and

sampling the data stream using the selected one of the multiphase signals to produce a retimed data signal.

2. The method of Claim 1 wherein said generating step generates multiphase clock signals which are subharmonics of the data stream.

3. The method of Claim 1 wherein said selecting step includes the step of determining whether the multiphase clock signals are either early or late with respect to the data stream.

4. The method of Claim 3 wherein said determining step includes the further step of sampling the multiphase clock signals using a plurality of D-type flip-flops.

5. The method of Claim 1 wherein:

each of the multiphase clock signals has at least one rising edge; and

said selecting step includes the step of using the synchronization states to define which of the rising edges of the multiphase clock signals is most closely aligned with an edge of the data stream.

6. The method of Claim 1 wherein said generating step generates the multiphase clock signals using a multiphase voltage-controlled oscillator.

7. The method of Claim 6 further comprising the steps of:

creating an error signal using the multiphase clock signals and the data stream;

applying the error signal to a charge pump; and

correcting the multiphase clock signals using a control voltage output of the charge pump.

8. The method of Claim 1 wherein said selecting step includes the step of using the synchronization states to define a plurality of retime state signals.

9. The method of Claim 8 wherein said sampling step further comprises the steps of:

inverting the multiphase clock signals to produce inverted phase signals;

combining respective pairs of the retime state signals and the inverted phase signals using a plurality of respective AND gates;

combining the outputs of the AND gates using an OR gate; and

latching the output of the OR gate using the data stream to produce the retimed data signal.

10. A circuit for effectively extracting a clock signal from a data stream, comprising:

means for generating a plurality of multiphase clock signals;

means for selecting one of the multiphase signals based on a plurality of synchronization states identifying which of the multiphase clock signals is most closely aligned with the data stream; and

means for sampling the data stream using the selected one of the multiphase signals to produce a retimed data signal.

11. The circuit of Claim 10 wherein said generating means generates multiphase clock signals which are subharmonics of the data stream.

12. The circuit of Claim 10 wherein said selecting means includes means for determining whether the multiphase clock signals are either early or late with respect to the data stream.

13. The circuit of Claim 12 wherein said determining means samples the multiphase clock signals using a plurality of D-type flip-flops.

14. The circuit of Claim 10 wherein:

each of the multiphase clock signals has at least one rising edge; and

said selecting means uses the synchronization states to define which of the rising edges of the multiphase clock signals is most closely aligned with an edge of the data stream.

15. The circuit of Claim 10 wherein said generating means includes a multiphase voltage-controlled oscillator.

16. The circuit of Claim 15 further comprising:

means for creating an error signal using the multiphase clock signals and the data stream; and

a charge pump receiving the error signal as an input, and providing a control voltage output to said voltage-controlled oscillator.

17. The circuit of Claim 10 wherein said selecting means uses the synchronization states to define a plurality of retime state signals.

18. The circuit of Claim 17 wherein said sampling means:

inverts the multiphase clock signals to produce inverted phase signals;

combines respective pairs of the retime state signals and the inverted phase signals using a plurality of respective AND gates;

further combines outputs of said AND gates using an OR gate; and

latches an output of said OR gate using the data stream to produce the retimed data signal.